Lab Experiment #3

ECE 282 - 002

Friday PM Lab

Carlos Sanchez and Connor Raasch

**Laboratory Experiment #3**

1. Work ‘Supplement to Experiment 2’ on p.600. Enter files found for HDL Example 3.3 on pp.130 and 132. You will use ‘Project Navigator’ to compile and simulate the circuit. Demonstrate your simulation to the TA. It should be similar to that shown in Fig. 3.38 on p.133. Include a copy of your Verilog files and simulation in your report.

timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 13:00:12 10/05/2018

// Design Name:

// Module Name: and\_or\_prop\_delay

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module and\_or\_prop\_delay(D,E,A,B,C);

input A,B,C;

output D,E;

wire w1;

and #30 G1(w1,A,B);

not #10 G2(E,C);

or #20 G3(D,w1,E);

endmodule

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 13:07:33 10/05/2018

// Design Name: and\_or\_prop\_delay

// Module Name: E:/ECE 282 lab/Lab3Part1/and\_or\_prop\_delay\_tb.v

// Project Name: Lab3Part1

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: and\_or\_prop\_delay

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module and\_or\_prop\_delay\_tb;

wire D,E;

reg A,B,C;

and\_or\_prop\_delay UUT (D, E, A, B, C);

initial begin

A = 1'b0; B = 1'b0; C=1'b0;

#100 A = 1'b1; B = 1'b1; C=1'b1;

end

initial #200 $finish;

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 16:04:56 10/16/2018

// Design Name:

// Module Name: and\_or\_prop\_delay

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module and\_or\_prop\_delay(D,E,A,B,C);

input A,B,C;

output D,E;

wire w1;

and #30 G1(w1,A,B);

not #10 G2(E,C);

or #20 G3(D,w1,E);

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 16:04:56 10/16/2018

// Design Name:

// Module Name: and\_or\_prop\_delay

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module and\_or\_prop\_delay\_tb;

wire D,E;

reg A,B,C;

and\_or\_prop\_delay UUT (D, E, A, B, C);

initial begin

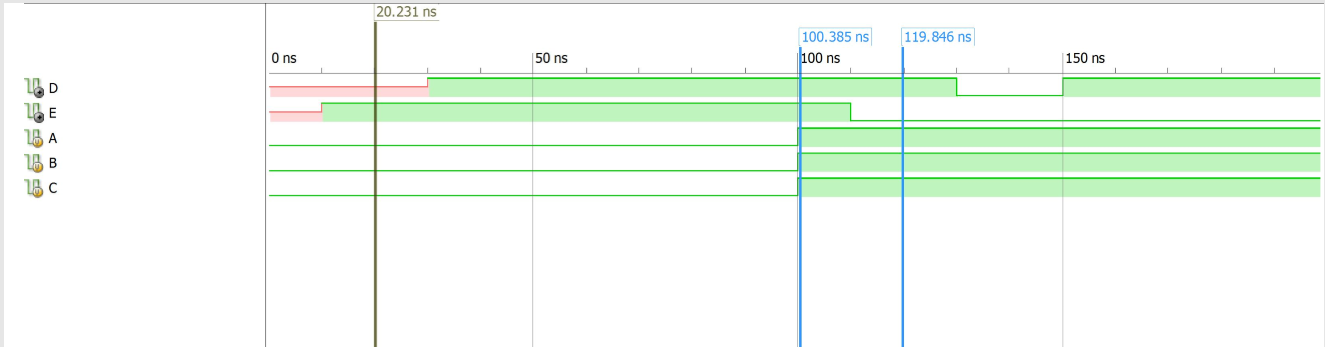
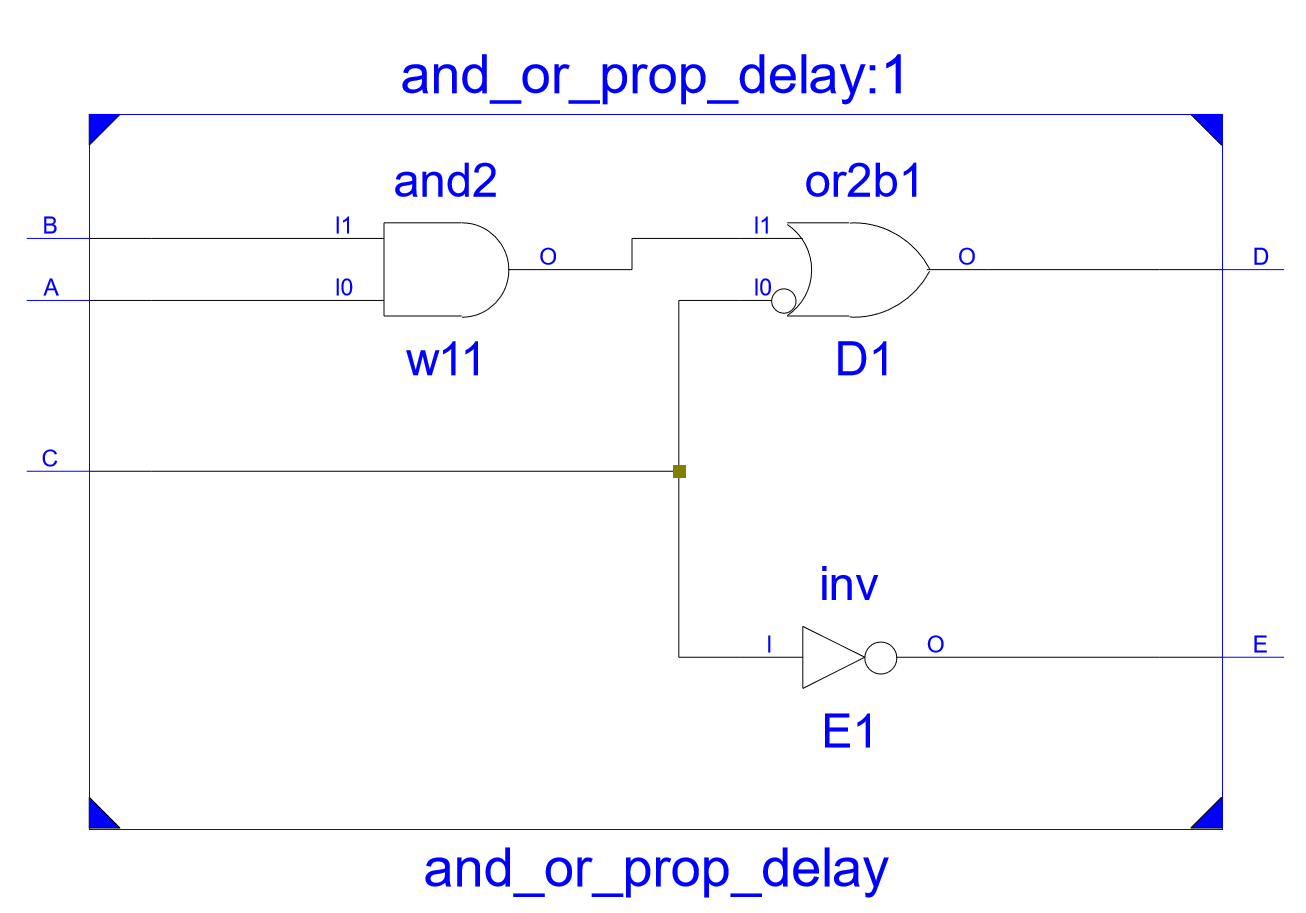
A = 1'b0; B = 1'b0; C=1'b0;

#100 A = 1'b1; B = 1'b1; C=1'b1;

end

initial #200 $finish;

endmodule



2. Continue with ‘Supplement to Experiment 2’ by working parts a, b and c. The length of the simulation should be from t=0 to t=120ns instead of what is shown in the text. Demonstrate your simulation to the TA. Include a copy of your Verilog files and simulation in your report.

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 16:33:09 10/09/2018

// Design Name:

// Module Name: XOR\_gate

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module xor\_and\_or\_not(F,X,Y)

input X,Y;

output F;

wire w1,w2,w3,w4;

not #10 G1(w1,x);

not #10 G2(w2,y);

and #20 G3(w3,x,w2);

and #20 G4(w4,y,w1);

or #30 G5 (F,w3,w4);

endmodule

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 16:40:21 10/09/2018

// Design Name: XOR\_gate

// Module Name: E:/Lab3Part2/XOR\_gate\_tb.v

// Project Name: Lab3Part2

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: XOR\_gate

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module XOR\_gate\_tb;

reg x, y;

wire Out;

XOR\_gate UUT (Out, x, y);

initial

begin

{x, y} = 0; #50;

{x, y} = 1; #50;

end

initial #120 $finish;

Endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 15:44:16 10/16/2018

// Design Name:

// Module Name: XOR\_gate

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module xor\_and\_or\_not(F,A,B)

input A,B;

output F;

wire w1,w2,w3,w4;

not #10 G1(w1,A);

not #10 G2(w2,B);

and #20 G3(w3,A,w2);

and #20 G4(w4,B,w1);

or #30 G5 (F,w3,w4);

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 15:54:10 10/16/2018

// Design Name:

// Module Name: XOR\_gate

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module XOR\_gate\_tb;

reg A, B;

wire F;

XOR\_gate UUT (F, A, B);

initial

begin

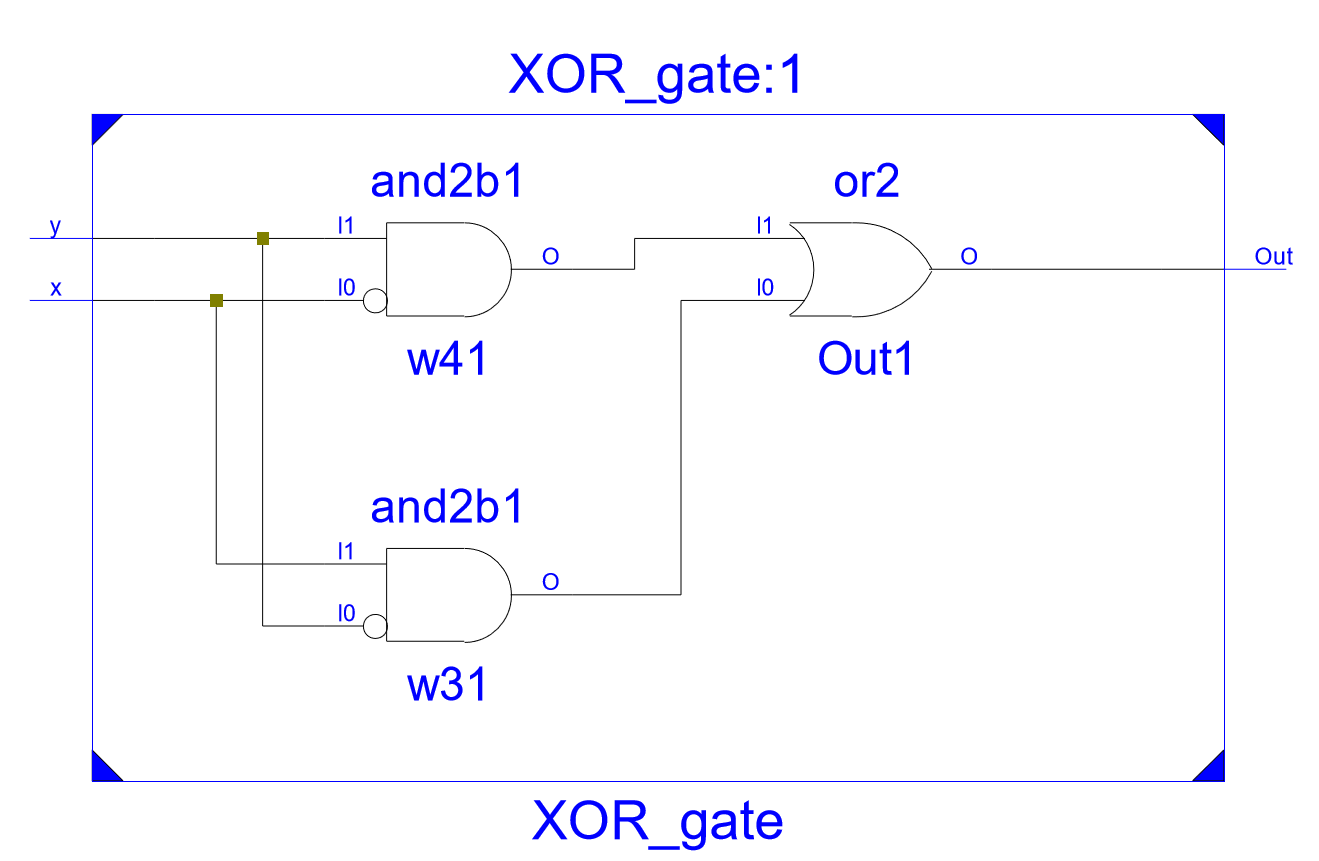
{A, B} = 0; #50;

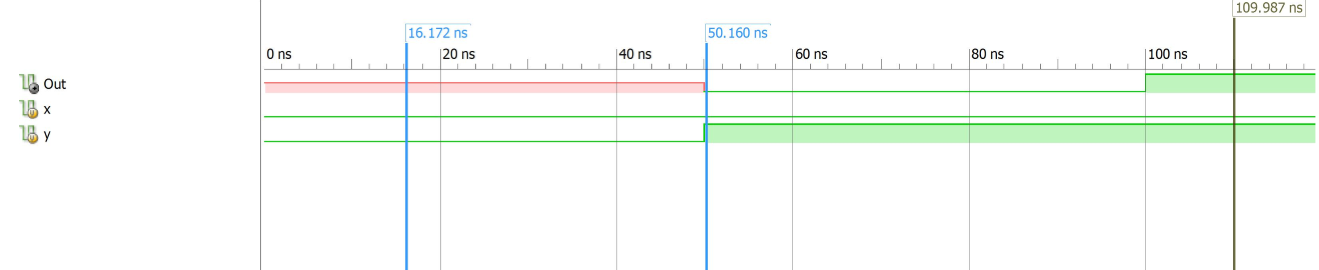
{A, B} = 1; #50;

end

initial #120 $finish;

endmodule





3. Work ‘Supplement to Experiment 4’ part a on p.601. Compile and simulate HDL Example 4.10 on p.219. Demonstrate your simulation to the TA showing that it provides the truth table for the circuit. Include a copy of your Verilog files and simulation in your report.

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 17:01:09 10/09/2018

// Design Name:

// Module Name: Mulitplex\_4x1

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module Mulitplex\_4x1(m\_out, in\_0, in\_1, in\_2, in\_3, select);

input in\_0, in\_1, in\_2, in\_3;

input [1:0] select;

output reg m\_out;

always @(in\_0, in\_1, in\_2, in\_3, select)

case (select)

2'b00: m\_out<=in\_0;

2'b01: m\_out<=in\_1;

2'b10: m\_out<=in\_2;

2'b11: m\_out<=in\_3;

endcase

endmodule

---------------------------------------------------------------------------------------------------------------------

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 17:16:40 10/09/2018

// Design Name: Mulitplex\_4x1

// Module Name: E:/Lab3Part3/Mulitplex\_4x1\_tb.v

// Project Name: Lab3Part3

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: Mulitplex\_4x1

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module Mulitplex\_4x1\_tb;

reg in\_0, in\_1, in\_2, in\_3;

reg [1:0] select;

wire m\_out;

Mulitplex\_4x1 UUT (m\_out, in\_0, in\_1, in\_2, in\_3, select);

initial

begin

in\_0 = 1'b1; in\_1 = 1'b0; in\_2 = 1'b0; in\_3 = 1'b0; select = 2'b00; #10;

in\_0 = 1'b0; in\_1 = 1'b1; in\_2 = 1'b0; in\_3 = 1'b0; select = 2'b01; #10;

in\_0 = 1'b0; in\_1 = 1'b0; in\_2 = 1'b1; in\_3 = 1'b0; select = 2'b10; #10;

in\_0 = 1'b0; in\_1 = 1'b0; in\_2 = 1'b0; in\_3 = 1'b1; select = 2'b11; #10;

end

initial #40 $finish;

Endmodule

---------------------------------------------------------------------------------------------------------------------

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 18:14:50 10/16/2018

// Design Name:

// Module Name: and\_or\_prop\_delay

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module Mulitplex\_4x1(m\_out, in\_0, in\_1, in\_2, in\_3, select);

input in\_0, in\_1, in\_2, in\_3;

input [1:0] select;

output reg m\_out;

always @(in\_0, in\_1, in\_2, in\_3, select)

case (select)

2'b00: m\_out<=in\_0;

2'b01: m\_out<=in\_1;

2'b10: m\_out<=in\_2;

2'b11: m\_out<=in\_3;

endcase

Endmodule

---------------------------------------------------------------------------------------------------------------------

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 18:16:36 10/16/2018

// Design Name:

// Module Name: Mulitplex\_4x1

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module Mulitplex\_4x1\_tb;

reg in\_0, in\_1, in\_2, in\_3;

reg [1:0] select;

wire m\_out;

Mulitplex\_4x1 UUT (m\_out, in\_0, in\_1, in\_2, in\_3, select);

initial

begin

in\_0 = 1'b1; in\_1 = 1'b0; in\_2 = 1'b0; in\_3 = 1'b0; select = 2'b00; #10;

in\_0 = 1'b0; in\_1 = 1'b1; in\_2 = 1'b0; in\_3 = 1'b0; select = 2'b01; #10;

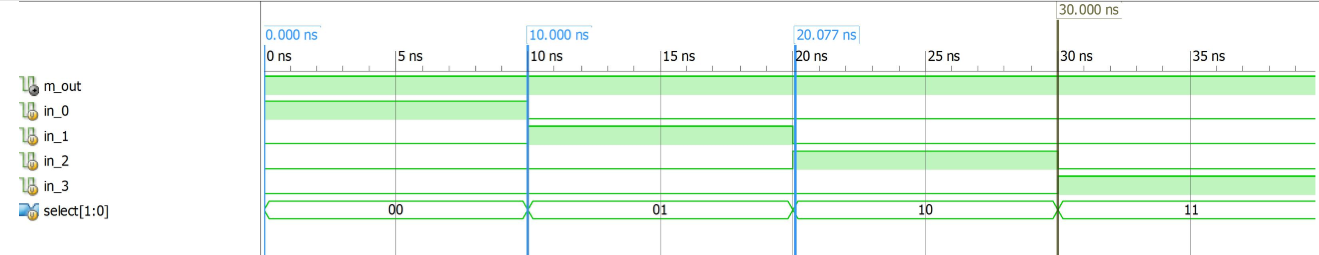
in\_0 = 1'b0; in\_1 = 1'b0; in\_2 = 1'b1; in\_3 = 1'b0; select = 2'b10; #10;

in\_0 = 1'b0; in\_1 = 1'b0; in\_2 = 1'b0; in\_3 = 1'b1; select = 2'b11; #10;

end

initial #40 $finish;

endmodule



4. Continue with ‘Supplement to Experiment 4’ part b on p.602. Use Verilog to compile and simulate the three-input Majority Circuit that was completed in the pre-lab. Demonstrate your

simulation to the TA. Include a copy of your Verilog files and simulation in your report.

timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 17:30:45 10/09/2018

// Design Name:

// Module Name: Majority\_3x1

// Project Name:

// Target Device:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module Majority\_3x1(Out,x,y,z,)

input x,y,z;

output Out;

wire w1,w2,w3;

and G1(w1,x,z);

and G2(w2,y,z);

and G3(w3,x,y);

or G4(Out,w1,w2,w3);

endmodule

timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Connor Raasch

//

// Create Date: 17:35:32 10/09/2018

// Design Name: Majority\_3x1

// Module Name: E:/Lab3Part4/Majority\_3x1\_tb.v

// Project Name: Lab3Part4

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: Majority\_3x1

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module Majority\_3x1\_tb;

reg x, y, z;

wire Out;

Majority\_3x1 UUT (Out, x, y, z);

initial

begin

x = 1'b0; y = 1'b0; z = 1'b0; #10;

x = 1'b0; y = 1'b0; z = 1'b1; #10;

x = 1'b0; y = 1'b1; z = 1'b0; #10;

x = 1'b0; y = 1'b1; z = 1'b1; #10;

x = 1'b1; y = 1'b0; z = 1'b0; #10;

end

initial #70 $finish;

endmodule

---------------------------------------------------------------------------------------------------------------------

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 17:03:26 10/16/2018

// Design Name:

// Module Name: Majority\_3x1

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module Majority\_Circ(F,x,y,z,)

input x,y,z;

output F;

wire w1,w2,w3;

and G1(w1,x,z);

and G2(w2,y,z);

and G3(w3,x,y);

or G4(F,w1,w2,w3);

endmodule

---------------------------------------------------------------------------------------------------------------------

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer: Carlos Sanchez

//

// Create Date: 17:04:46 10/16/2018

// Design Name:

// Module Name: Majority\_3x1

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

// ECE 282 - 002

//

//////////////////////////////////////////////////////////////

module Majority\_Circ\_tb;

reg x, y, z;

wire F;

Majority\_Circ UUT (F, x, y, z);

initial

begin

x = 1'b0; y = 1'b0; z = 1'b0; #10;

x = 1'b0; y = 1'b0; z = 1'b1; #10;

x = 1'b0; y = 1'b1; z = 1'b0; #10;

x = 1'b0; y = 1'b1; z = 1'b1; #10;

x = 1'b1; y = 1'b0; z = 1'b0; #10;

end

initial #70 $finish;

endmodule

